BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

IN THE CLAIMS:

Kindly amend claim 1 as follows:

C3

1. (Twice Amended) A complementary MOS semiconductor device, comprising: a semiconductor substrate; a CMOS transistor pair comprised of an N-channel MOS transistor formed in the semiconductor substrate and a P-channel MOS transistor formed in the semiconductor substrate, the N-channel MOS transistor and the P-channel MOS transistor forming a complementary transistor pair; and a resistor formed in the semiconductor substrate; wherein a conductivity type of a gate electrode of the N-channel MOS transistor is P-type, and a conductivity type of a gate electrode of the P-channel MOS transistor is P-type.

Kindly add the following new claims 74-93:

C4

74. A complementary MOS semiconductor device according to claim 1; wherein the P-type gate electrode of the N-channel MOS transistor and the P-type gate electrode of the P-channel MOS transistor each comprise a single layer of polycrystalline silicon.

75. A complementary MOS semiconductor device according to claim 74; wherein film thickness of the polycrystalline silicon layer is in the range of 2000 angstroms to 6000 angstroms.

76. A complementary MOS semiconductor device according to claim 74; wherein the polycrystalline silicon layer has a concentration of boron or BF_2 in a concentration of at least 1 x 10^{19} atoms/cm^3.

77. A complementary MOS semiconductor device according to claim 1; wherein the P-type gate electrode of the N-channel MOS transistor and the P-type gate electrode of the P-channel MOS transistor each comprise a polycide structure comprising a polycrystalline silicon layer and a high melting point metal silicide layer formed thereover.

78. A complementary MOS semiconductor device according to claim 77; wherein the high melting point metal silicide layer is formed of at least one metal silicide selected from the group consisting of molybdenum silicide, tungsten silicide, titanium silicide and platinum silicide.

79. A complementary MOS semiconductor device according to claim 77; wherein the high melting point metal silicide layer has a thickness in the range of 500 angstroms to 2500 angstroms.

80. A complementary MOS semiconductor device according to claim 77; wherein the resistor is a polycrystalline silicon resistor formed from the same polycrystalline silicon layer and having the same thickness as

that of the polycrystalline silicon layer of the gate electrodes of the N-channel MOS transistor and the P-channel MOS transistor.

81. A complementary MOS semiconductor device according to claim 77; wherein the resistor is a polycrystalline silicon resistor formed of a polycrystalline silicon film having a thickness in the range of 500 angstroms to 2000 angstroms.

82. A complementary MOS semiconductor device according to claim 77; wherein the resistor is a thin film transistor.

c4

83. A complementary MOS semiconductor device according to claim 1; wherein the P-channel MOS transistor is an enhancement mode transistor having a surface channel.

84. A complementary MOS semiconductor device according to claim 83; wherein the P-channel MOS transistor has a threshold voltage of approximately -0.5V.

85. A complementary MOS semiconductor device according to claim 84; wherein the N-channel MOS transistor is an enhancement mode transistor having a buried channel.

86. A complementary MOS semiconductor device according to claim 85; wherein a threshold voltage of the N-channel MOS transistor is set using arsenic as a donor impurity so that the buried channel is a shallow buried channel.

87. A complementary MOS semiconductor device according to claim 1; wherein the N-channel MOS transistor is used in a reference voltage generating circuit of a voltage regulator and the P-channel MOS transistor is used as an output driving transistor of the voltage regulator.

C4

88. A complementary MOS semiconductor device for a voltage regulator, comprising: a semiconductor substrate; an N-channel MOS transistor formed in the semiconductor substrate and used in a reference voltage generating circuit of the voltage regulator; a P-channel MOS transistor formed in the semiconductor substrate and used as an output element of the voltage regulator; and a resistor formed in the semiconductor substrate; wherein a conductivity type of a gate electrode of the N-channel MOS transistor is P-type, and a conductivity type of a gate electrode of the P-channel MOS transistor is P-type.

89. A complementary MOS semiconductor device for a voltage regulator having a reference voltage generating circuit, an error amplifier, an output driving transistor and

a voltage divider, the complementary MOS semiconductor device comprising: a semiconductor substrate; a complementary transistor pair comprised of an N-channel MOS transistor formed in the semiconductor substrate and a P-channel MOS transistor formed in the semiconductor substrate, one of the complementary transistors serving as the output driving transistor of the voltage regulator; and a resistor formed in the semiconductor substrate and used in the voltage divider; wherein a conductivity type of a gate electrode of the N-channel MOS transistor is P-type, and a conductivity type of a gate electrode of the P-channel MOS transistor is P-type.

C4

90. A complementary MOS semiconductor device according to claim 89; wherein the P-channel MOS transistor is an enhancement mode transistor having a surface channel.

91. A complementary MOS semiconductor device according to claim 90; wherein the P-channel MOS transistor has a threshold voltage of approximately -0.5V.

92. A complementary MOS semiconductor device according to claim 91; wherein the N-channel MOS transistor is an enhancement mode transistor having a buried channel.

C4

93. A complementary MOS semiconductor device according to claim 92; wherein a threshold voltage of the N-channel MOS transistor is set using arsenic as a donor impurity so that the buried channel is a shallow buried channel.

ADDITIONAL FEES:

A check in the amount of $360.00 is enclosed to cover the cost of 16 claims in excess of those already paid for. Should the check prove insufficient for any reason, authorization is hereby given to charge any such deficiency to our Deposit Account No. 01-0268.

REMARKS

This supplemental response is being filed for the purpose of broadening amended independent claim 1 and adding new claims 74-93, including dependent claims 74-87 and 90-93 and independent claims 88 and 89. Independent claim 88 is identical to amended claim 1 as set forth in the last-filed response. Independent claim 89 is a somewhat broadened version of claim 88. In addition, the specification has been revised in minor additional respects to correct informalities.

As recited by amended independent claims 1, 88 and 89, the CMOS device of the present invention has an N-channel MOS transistor and a P-channel MOS transistor, each having a